

What is claimed is:

- 1        1.    A method comprising:  
2        determining whether execution of an instruction of a  
3        first thread may require a long latency; and  
4        switching to a second thread if the instruction may  
5        require the long latency.
  
- 1        2.    The method of claim 1, further comprising  
2        executing at least one additional instruction in the first  
3        thread while preparing to switch to the second thread.
  
- 1        3.    The method of claim 1, wherein the determining is  
2        based on a stochastic analysis of whether the instruction  
3        will result in a long latency.
  
- 1        4.    The method of claim 1, wherein the determining  
2        comprises applying the instruction to a lookup table in a  
3        processor pipeline.
  
- 1        5.    The method of claim 4, further comprising  
2        providing a feedback signal from an instruction decoder to  
3        an instruction fetch unit to switch to the second thread.
  
- 1        6.    The method of claim 1, wherein the long latency  
2        comprises less than ten processor cycles.

1           7.    The method of claim 1, further comprising  
2   switching back to the first thread.

1           8.    A method comprising:  
2           switching from a first thread to a second thread if a  
3   condition that may result in a stall of a processor  
4   pipeline occurs during execution of the first thread in the  
5   processor pipeline.

1           9.    The method of claim 8, further comprising  
2   determining whether the condition occurs by comparing an  
3   instruction to entries in a lookup table.

1           10.   The method of claim 8, further comprising  
2   executing at least one additional instruction after the  
3   condition occurs and before switching to the second thread.

1           11.   The method of claim 8, wherein the condition is  
2   based on a stochastic model.

1           12.   The method of claim 8, further comprising  
2   providing a feedback signal from an instruction decoder to  
3   an instruction fetch unit to switch to the second thread.

1        13. An article comprising a machine-readable storage  
2 medium containing instructions that if executed enable a  
3 system to:

4        switch from a first thread to a second thread if a  
5 condition that may result in a stall of a processor  
6 pipeline occurs during execution of the first thread in the  
7 processor pipeline.

1        14. The article of claim 13, further comprising  
2 instructions that if executed enable the system to  
3 determine whether the condition occurs by comparing an  
4 instruction to entries in a lookup table.

1        15. The article of claim 13, further comprising  
2 instructions that if executed enable the system to execute  
3 at least one additional instruction in the first thread  
4 while the system prepares to switch to the second thread.

1        16. The article of claim 13, further comprising  
2 instructions that if executed enable the system to send a  
3 feedback signal to cause the switch from the first thread  
4 to the second thread.

1        17. An apparatus comprising:  
2        a processor pipeline having a feedback loop to provide  
3 a feedback signal to cause the processor pipeline to switch

4 from a first thread to a second thread, the feedback signal  
5 to originate from a location in the processor pipeline  
6 before instruction execution.

1 18. The apparatus of claim 17, wherein the feedback  
2 signal is coupled between an instruction decoder and an  
3 instruction fetch unit.

1 19. The apparatus of claim 18, wherein the  
2 instruction decoder is coupled to provide the feedback  
3 signal to the instruction fetch unit when a predetermined  
4 condition occurs.

1 20. The apparatus of claim 19, wherein the  
2 instruction decoder includes logic to determine when the  
3 predetermined condition occurs.

1 21. The apparatus of claim 19, wherein the  
2 instruction decoder includes a lookup table that includes a  
3 list of predetermined conditions.

1 22. A system comprising:  
2 a processor pipeline having a feedback loop to provide  
3 a feedback signal to cause the processor pipeline to switch  
4 from a first thread to a second thread, the feedback signal

5 to originate from a location in the processor pipeline  
6 before instruction execution; and  
7 a wireless interface coupled to the processor  
8 pipeline.

1 23. The system of claim 22, further comprising at  
2 least one storage device to store code to enable the  
3 processor pipeline to switch from the first thread to the  
4 second thread if a predetermined condition occurs during  
5 execution of the first thread.

1 24. The system of claim 23, wherein the at least one  
2 storage device includes code to enable the processor  
3 pipeline to execute at least one additional instruction in  
4 the first thread while the system prepares to switch to the  
5 second thread.

1 25. The system of claim 22, wherein the feedback  
2 signal is coupled between an instruction decoder and an  
3 instruction fetch unit.

1 26. The system of claim 25, wherein the instruction  
2 decoder is coupled to provide the feedback signal to the  
3 instruction fetch unit when a predetermined condition  
4 occurs.

1           27. The system of claim 26, wherein the instruction  
2 decoder includes logic to determine when the predetermined  
3 condition occurs.

1           28. The system of claim 26, wherein the instruction  
2 decoder includes a lookup table that includes a list of  
3 predetermined conditions.

1           29. The system of claim 22, wherein the wireless  
2 interface comprises a dipole antenna.